# Panel Discussion

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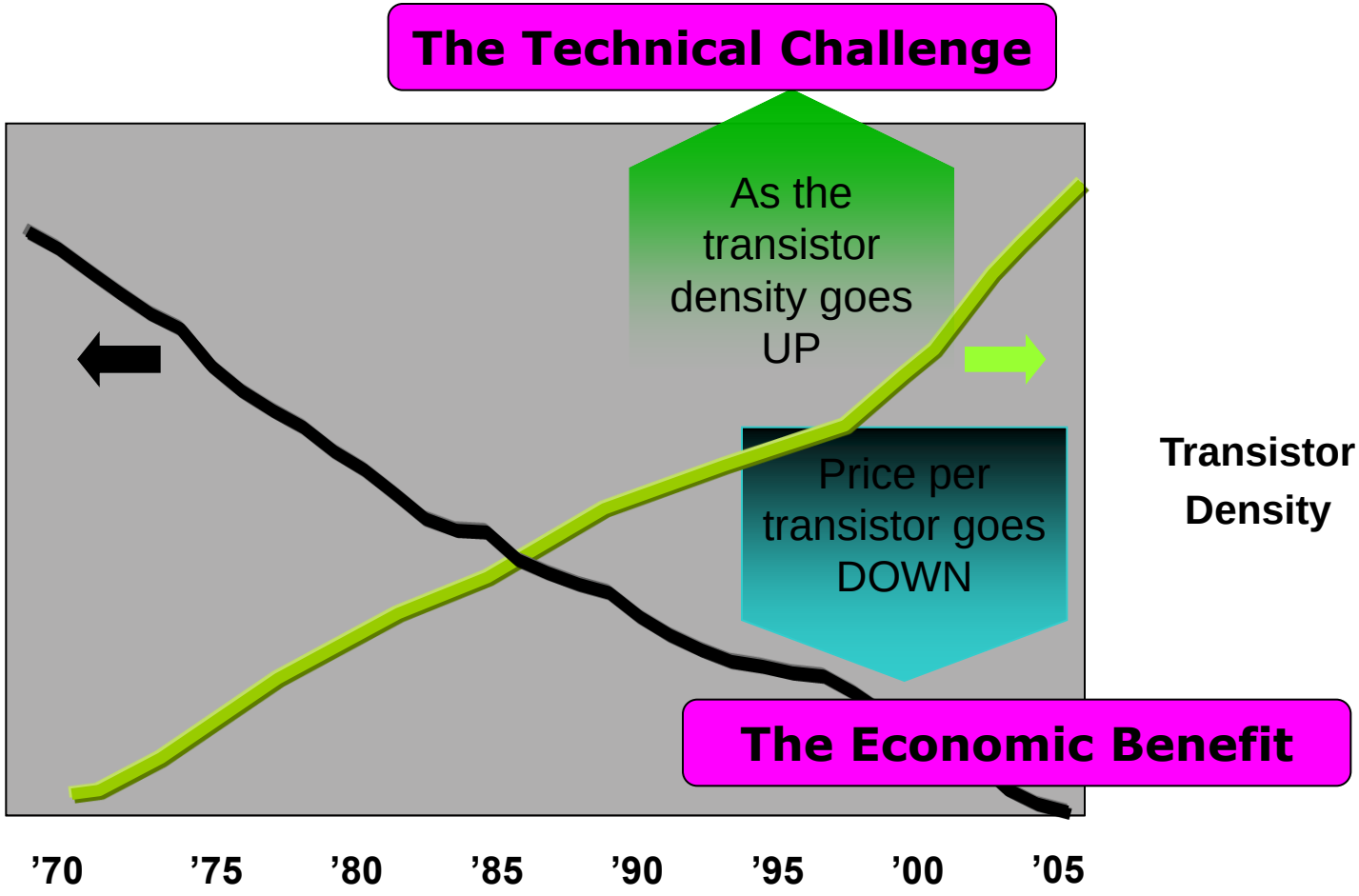
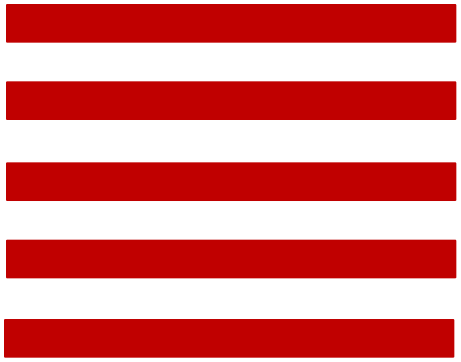
# The Bottom Line.....



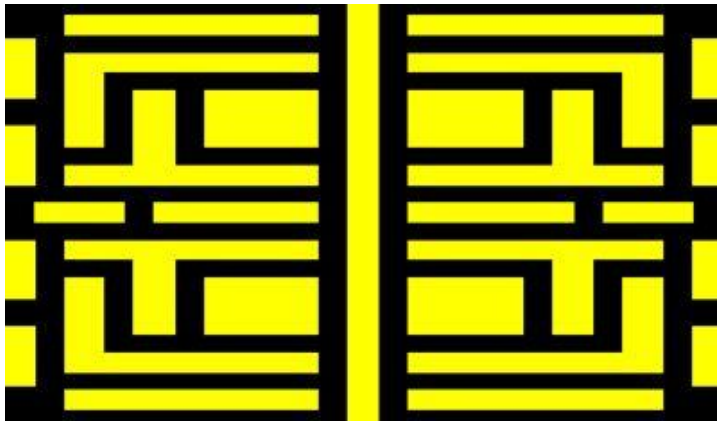

**Everything we do is a means to this end**

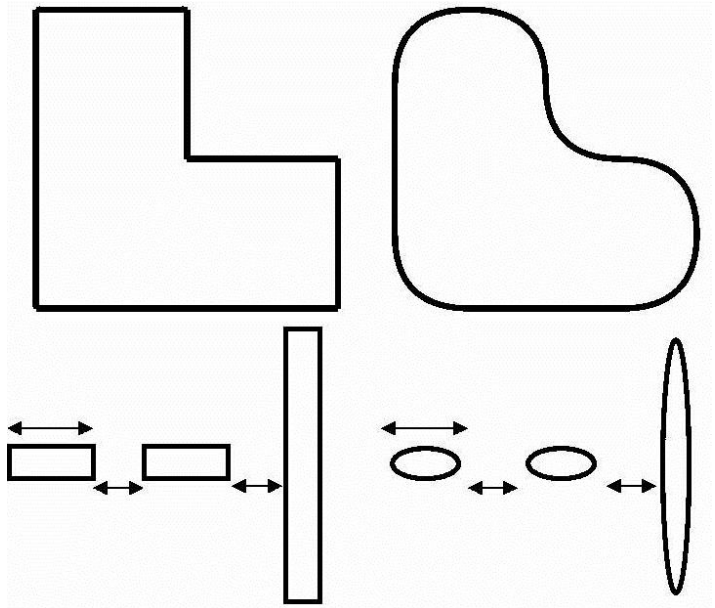
# 2D Structures Don't Scale Well

**Ideal Layout**



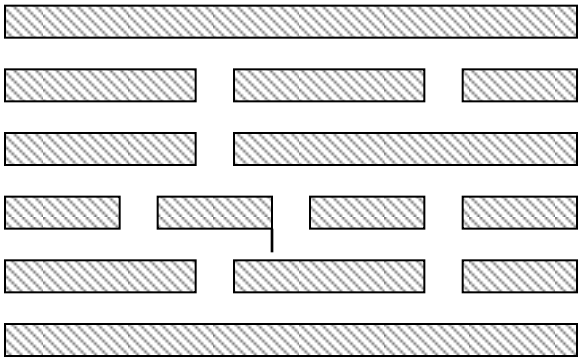
**Real Layout**

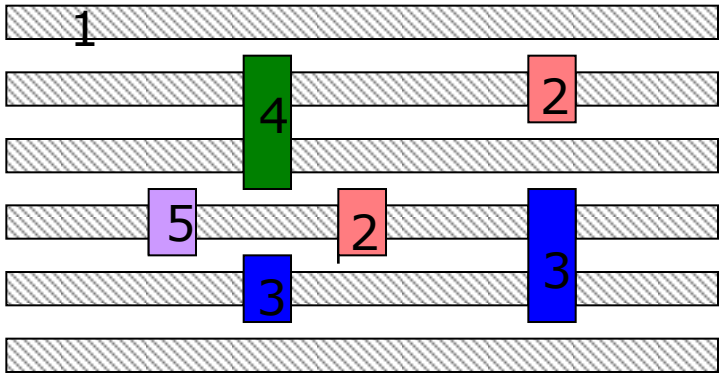




**The Outcome: An Explosion of Masks Required to achieve density**

# ArF Lithography

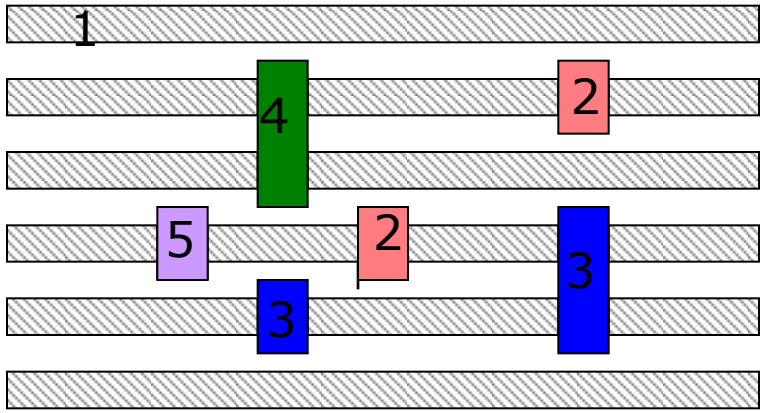




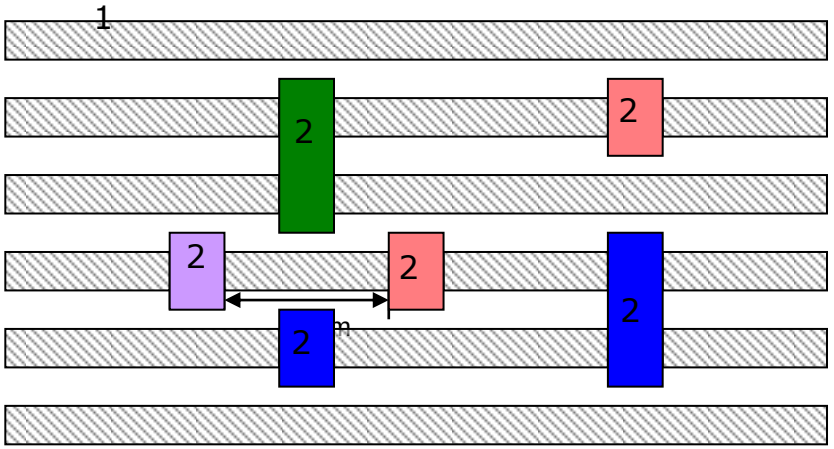

**1 Grating Mask**
**4 Cut Masks**
**Total: 5 Masks for 1 masking level**

**Affordability?**

# ArF MP vs. EUV




ArF: 5 masks

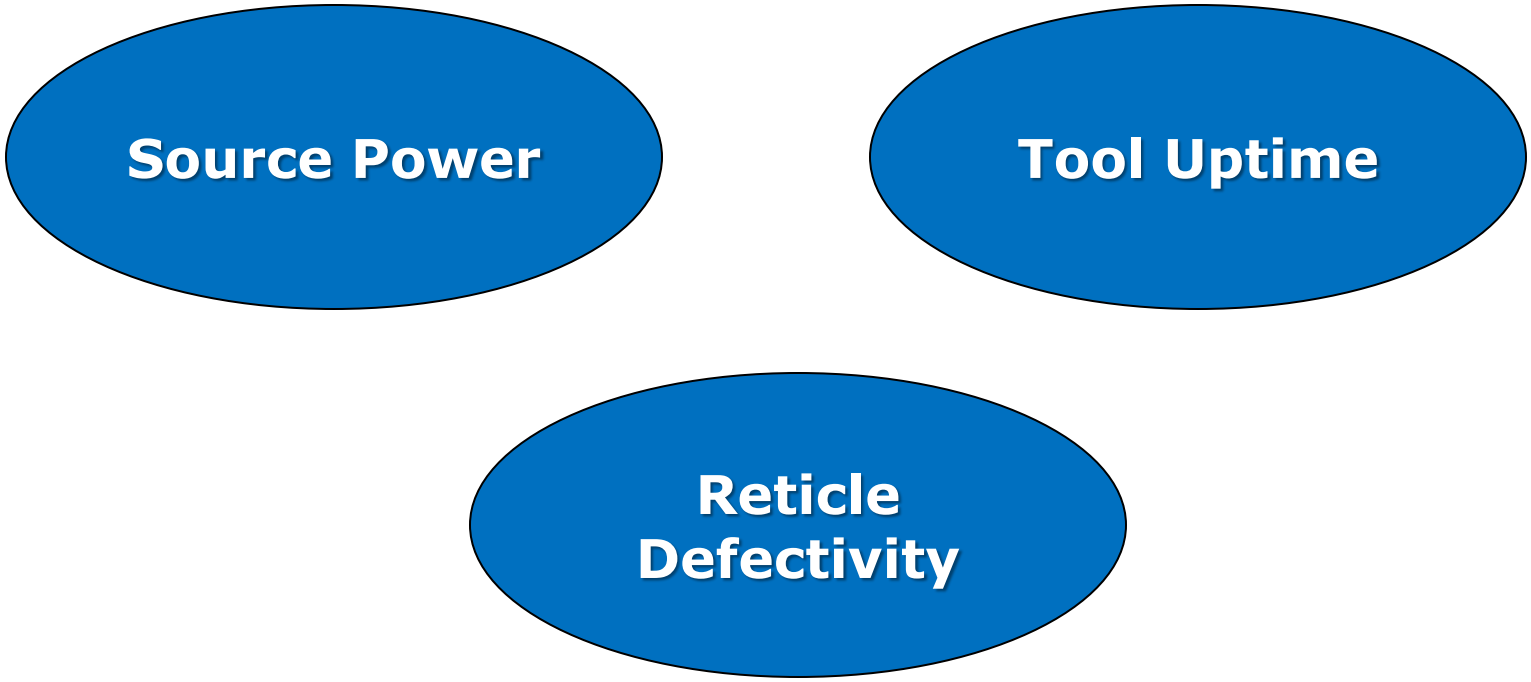



EUV: 2 masks

**Is 1 EUV exposure cheaper than 4 ArF exposures?**

**COO is what will determine EUV insertion timeline**

# The Keys for EUV




**Success in these areas is mandatory for favorable COO**

# $/Transistor

- Smaller features
  - Smaller chips, more die per wafer
  - More transistors per chip
- Cheaper wafers
  - Simpler processing
  - Fewer masks
  - Bigger wafers (450mm)

**Patterning technology is an means to the end**

**How do we deliver the lowest cost/transistor?**

# Implementation Strategy

- EUV currently targeted as primary option for 7nm node (2015 development, 2017 HVM)
- Are the key technical challenges going to be solved in time to deliver a COO less than ArF MP in this time frame?
- EUV and 450mm decisions are orthogonal
  - 300mm EUV tooling is 450mm compatible
  - EUV implementation will be on its own merits
  - If it can deliver a lower $/transistor, it will be in, regardless of node or wafer size
- It is our job to position EUV so that a clean data driven decision can be made to enable Moore's Law scaling to continue

# Thank You!